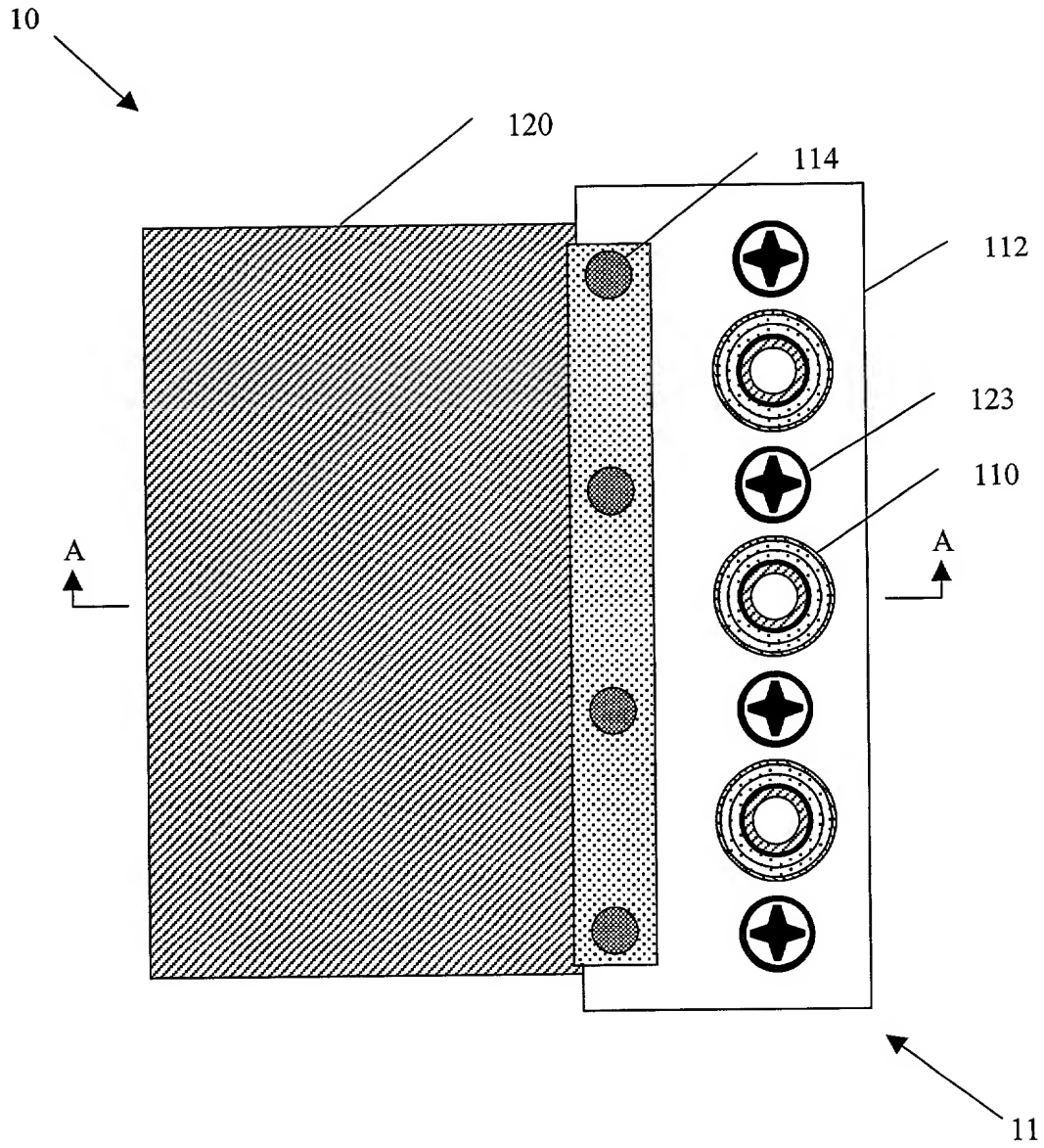
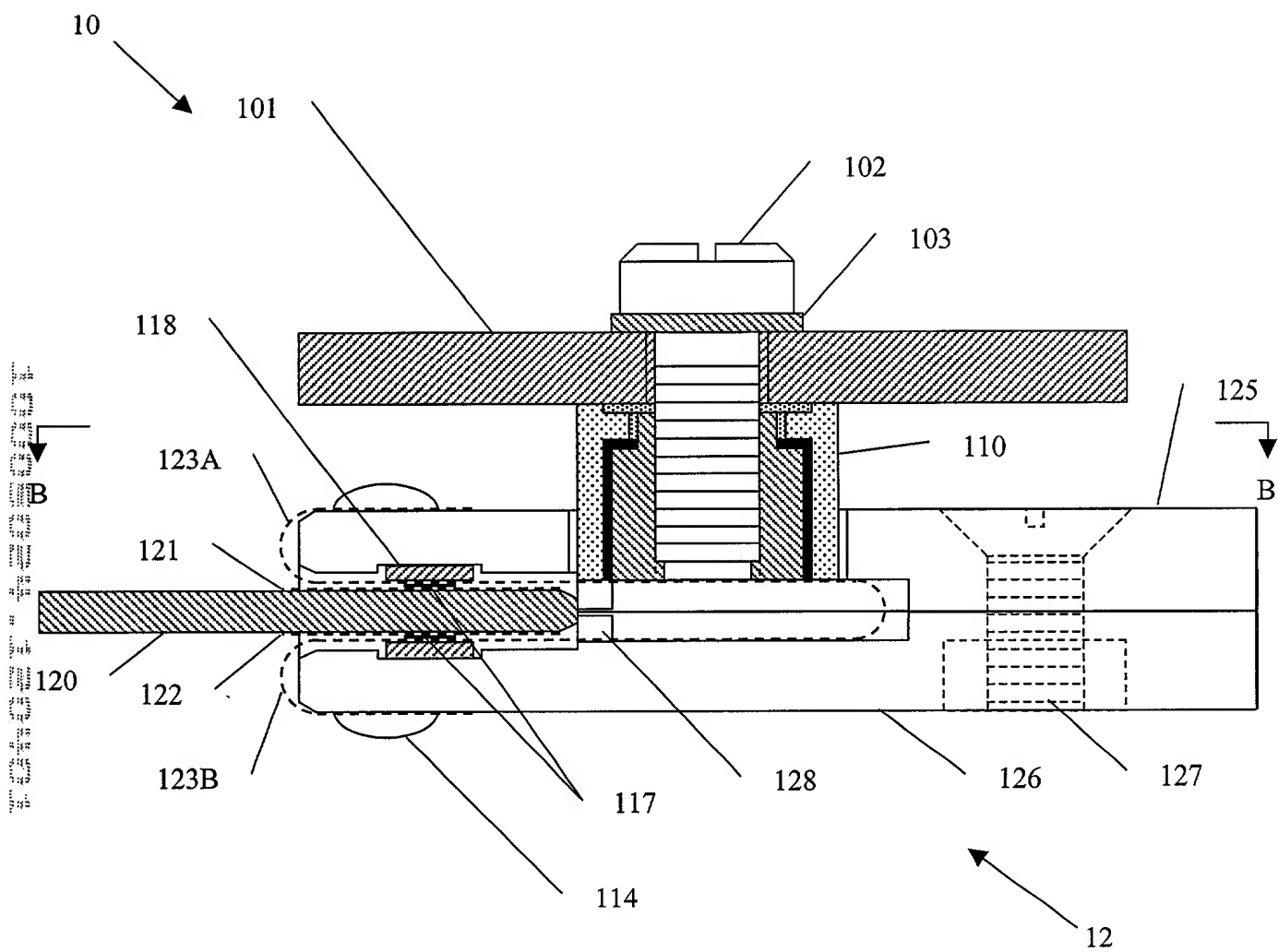


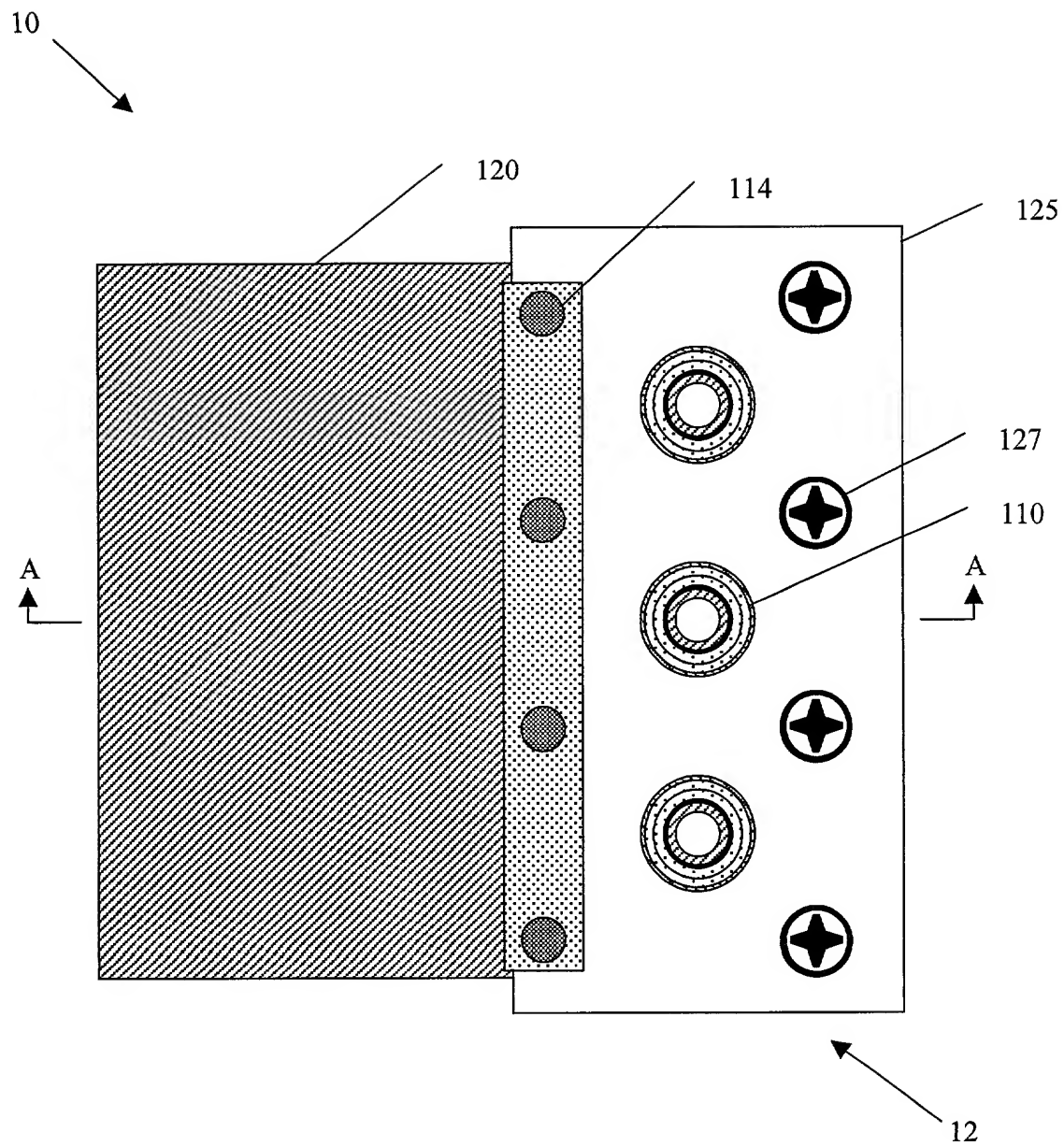
FIG. 1B is a cross-sectional view of the device 10 taken along line A-A of FIG. 1A. The device 10 includes a substrate 110, a first layer 112, a second layer 114, and a third layer 120. The first layer 112 is a conductive layer, the second layer 114 is a dielectric layer, and the third layer 120 is a conductive layer. The device 10 is formed on a substrate 110. The first layer 112 is formed on the substrate 110. The second layer 114 is formed on the first layer 112. The third layer 120 is formed on the second layer 114. The device 10 includes a plurality of openings 123 in the first layer 112. The openings 123 are filled with a conductive material 114. The device 10 is formed on a substrate 110. The first layer 112 is formed on the substrate 110. The second layer 114 is formed on the first layer 112. The third layer 120 is formed on the second layer 114. The device 10 includes a plurality of openings 123 in the first layer 112. The openings 123 are filled with a conductive material 114.



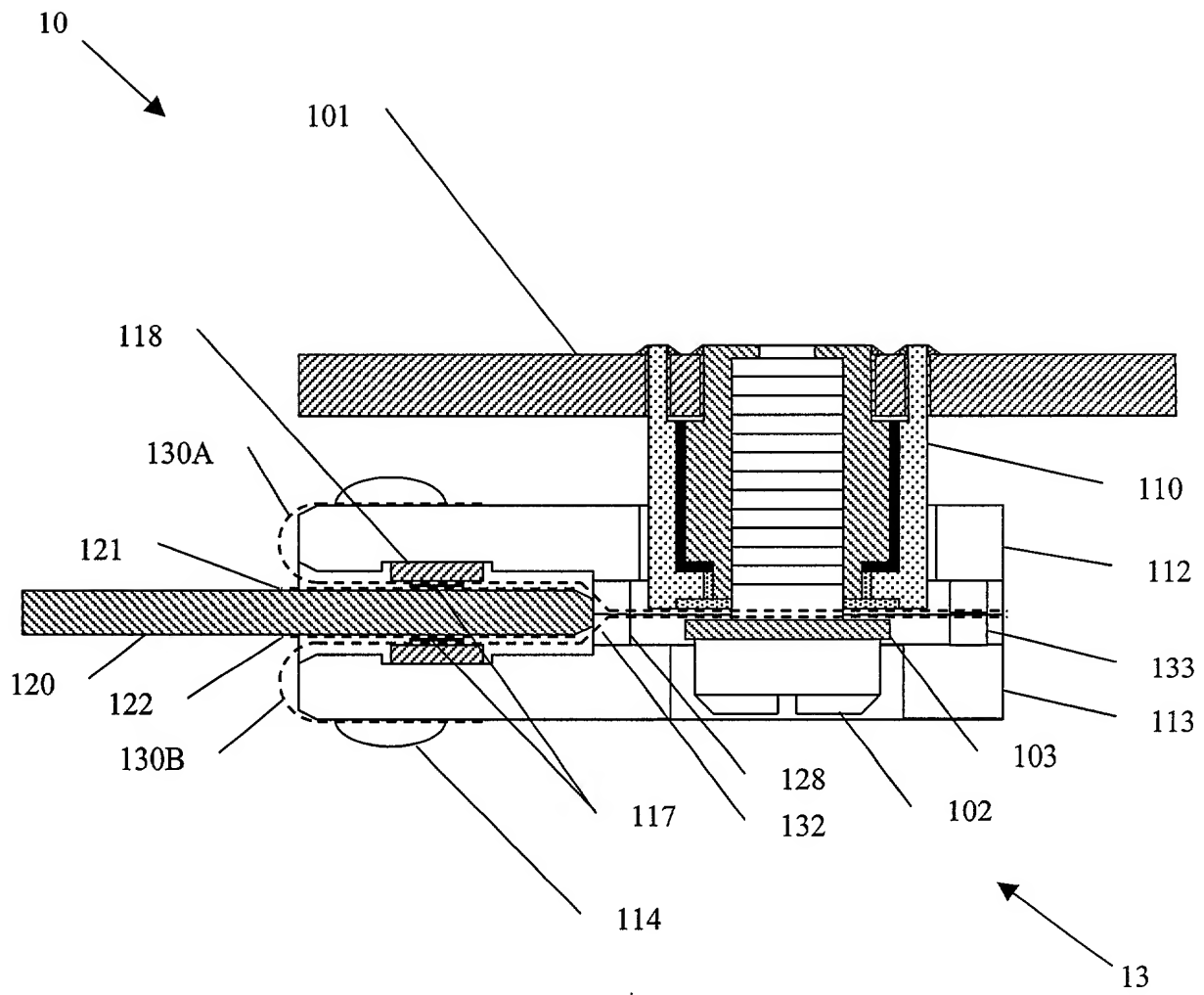
Section B-B
FIG. 1B



Section A-A
FIG. 2A

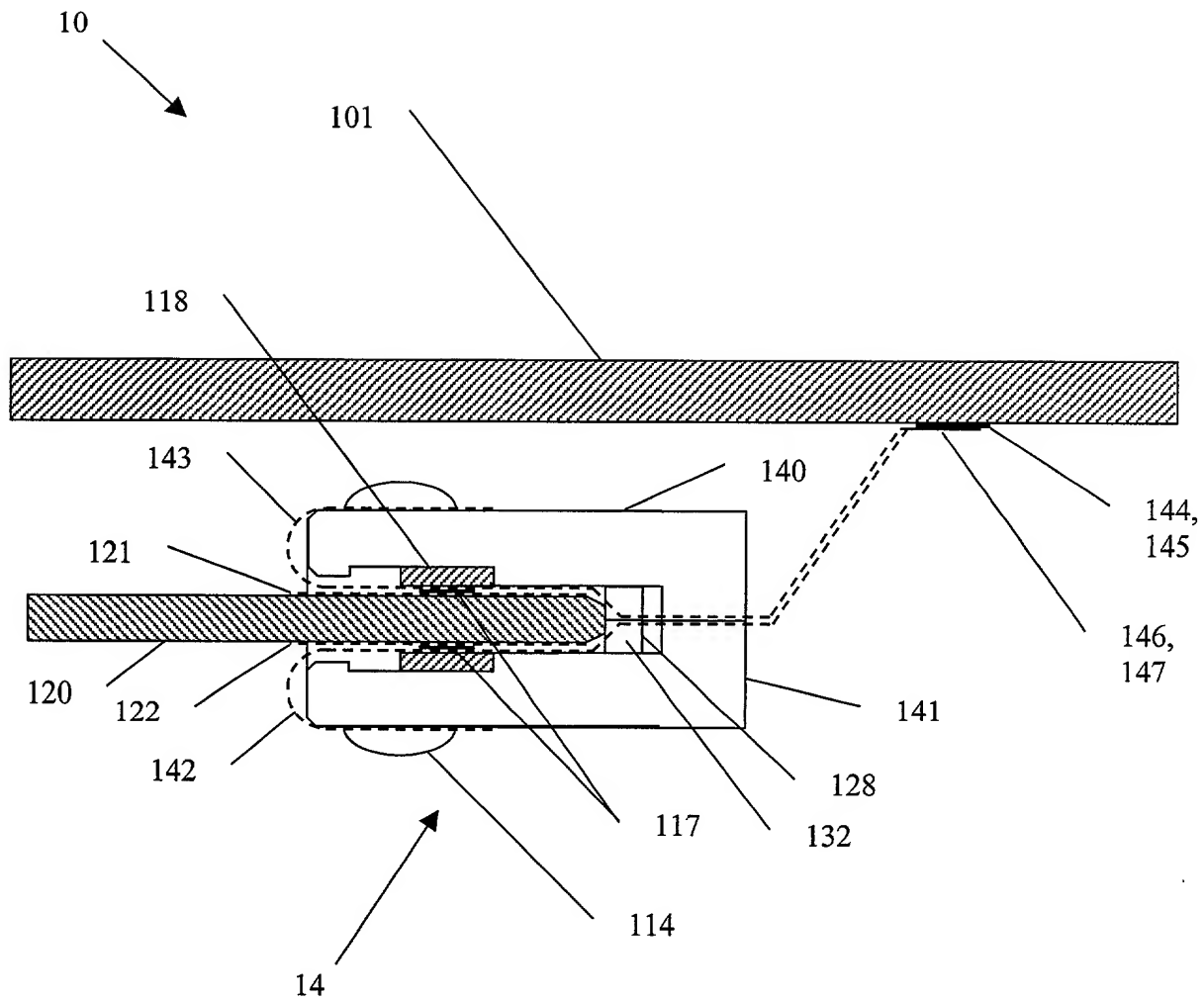


Section B-B
FIG. 2B



Section A-A
FIG. 3

FIG. 4A is a cross-sectional view of a device 10, taken along line A-A of FIG. 1. The device 10 includes a substrate 101, a gate stack 118, a gate electrode 121, a channel layer 120, a source/drain region 122, a contact layer 142, a contact pad 140, and a passivation layer 141. The contact pad 140 is electrically connected to the contact layer 142, which is electrically connected to the channel layer 120. The passivation layer 141 is disposed over the contact pad 140 and the contact layer 142. The gate stack 118 is disposed over the channel layer 120. The substrate 101 is disposed below the channel layer 120. The source/drain region 122 is disposed on the substrate 101. The contact layer 142 is disposed on the source/drain region 122. The contact pad 140 is disposed on the contact layer 142. The passivation layer 141 is disposed over the contact pad 140 and the contact layer 142. The gate stack 118 is disposed over the channel layer 120. The substrate 101 is disposed below the channel layer 120. The source/drain region 122 is disposed on the substrate 101. The contact layer 142 is disposed on the source/drain region 122. The contact pad 140 is disposed on the contact layer 142. The passivation layer 141 is disposed over the contact pad 140 and the contact layer 142.



Section A-A
FIG. 4A

10

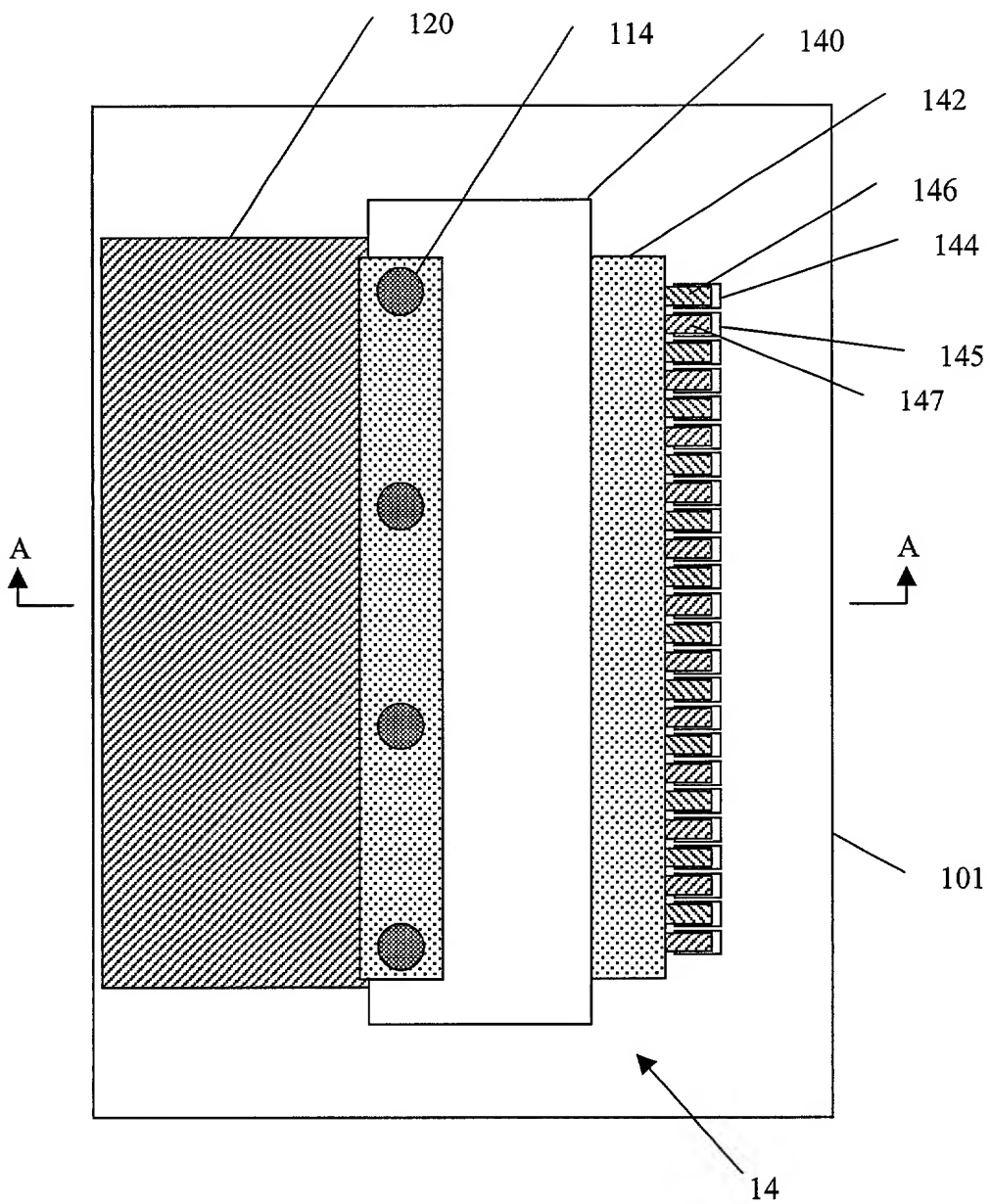


FIG. 4B

FIG. 5A is a schematic diagram of a device 100. The device 100 includes a substrate 110 and a plurality of components 115, 117, 502, 504, 508, 510, 514. The components 115, 117, 502, 504, 508, 510, 514 are arranged in a specific pattern on the substrate 110. The components 115, 117, 502, 504, 508, 510, 514 are arranged in a specific pattern on the substrate 110.

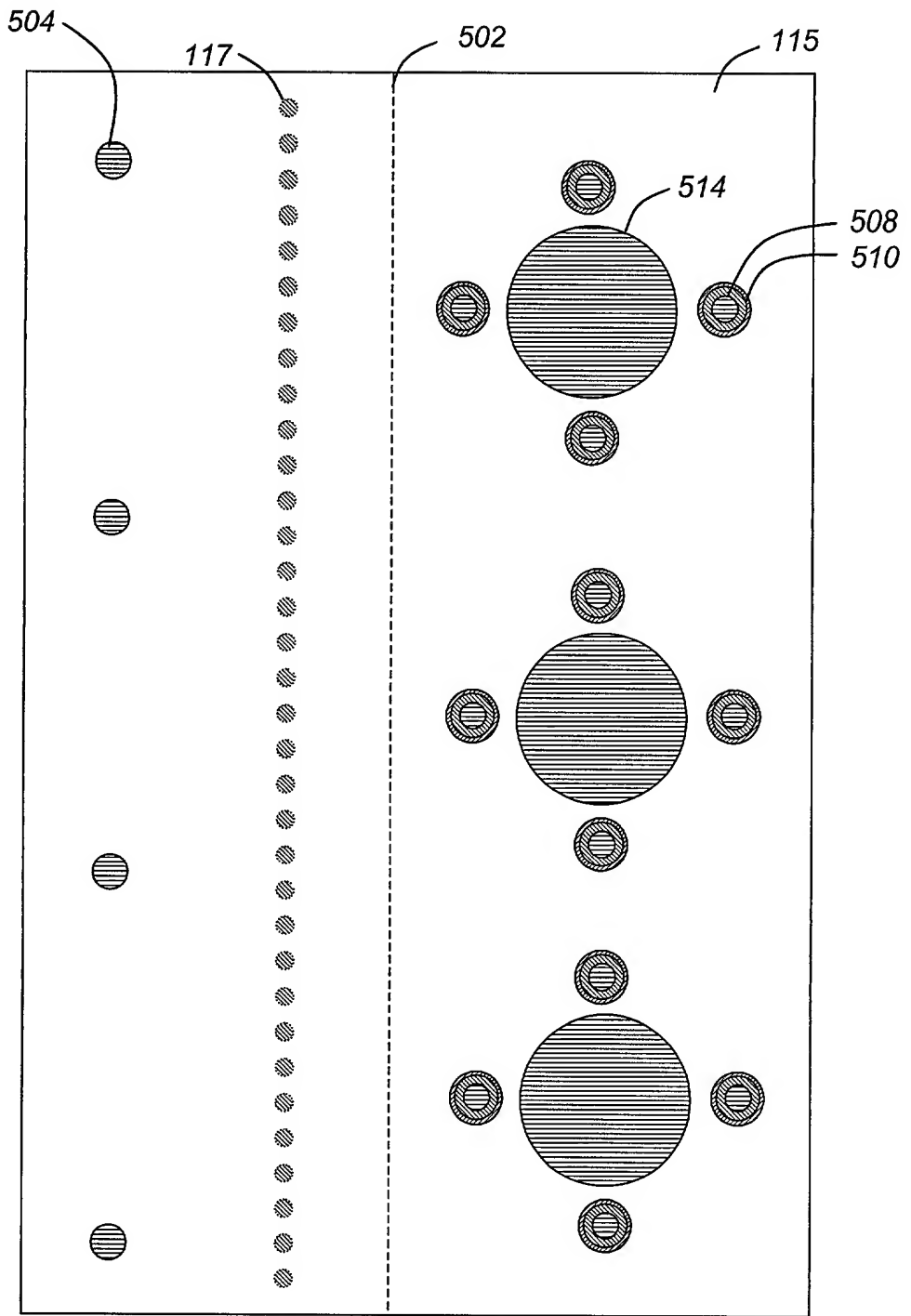


FIG. 5A

FIG. 5B is a schematic diagram of a device 100 in a second state. The device 100 is shown in a perspective view. The device 100 includes a substrate 116 and a plurality of elements 117. The elements 117 are arranged in a row. The elements 117 are connected to a common line 504. The elements 117 are connected to a common line 508. The elements 117 are connected to a common line 514. The elements 117 are connected to a common line 518.

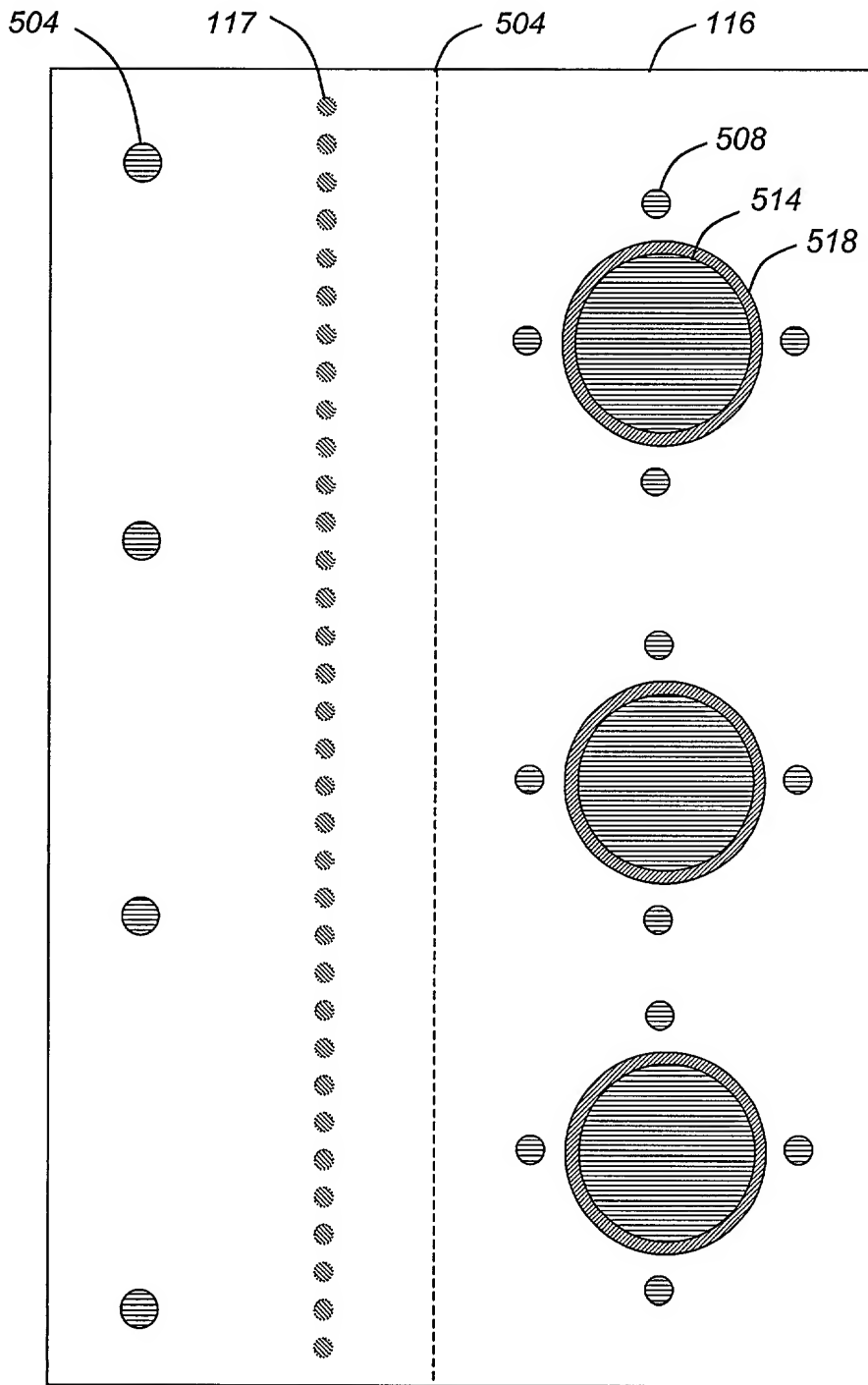


FIG. 5B